REMARKS

Claims 1-3 and 5-44 are pending, of which claims 1, 8, 18, and 27 are independent method claims, and claim 37 is an independent system claim. As shown above, claims 1, 8, and 37[1] have been amended by this paper, and claim 4[2] has been canceled without prejudice.

The Office Action rejected independent claims 1, 8, and 37 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,167,465 to Parvin et al. ("*Parvin*") and rejected independent claim 27 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,826,101 to Beck et al. ("*Beck*"). Each of the remaining dependent claims (with the exception of claim 13, which the Office Action indicated contains allowable subject matter) was rejected as anticipated by *Parvin* or *Beck*, or was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Parvin* or *Beck* in view of U.S. Patent No. 6,098,110 to Witkowski et al. ("*Witkowski*").[3]

The Office Action allowed claims 18-26. In response to the Examiner's statement of reasons for allowance, Applicants note for the record that it is the claimed combination of limitations that render these claims allowable, as opposed to an individual limitation read in isolation. Furthermore, particularly based on the remarks found below, Applicants respectfully submit that the allowed claims may have one or more additional independent bases for allowance that are not reflected in the Examiner's statement.

Applicants' invention, as claimed for example in independent method claim 1, relates to a method for arbitrating data requests, of one or more channels associated with one or more devices, to a main memory in a system having a direct memory access (DMA) engine with data reservoir storing channel data for the one or more channels. The method includes defining a circular list having a plurality of entries that correspond to the one or more channels. A channel associated with an entry in the circular list is evaluated to determine whether the channel requires service by (i) determining an entry time that represents how long until the channel will be

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[1]The Office Action objected to claim 37 based on inconsistent claim phraseology for interchanging the terms "DMA module" and "DMA engine" in the claim. Applicants have amended claim 37 to use only the term "DMA engine" to promote consistent claim terminology.

[2]Applicants note for the record that the subject matter of claim 4 has been incorporated into independent claim 1, and therefore does not evince an intent to surrender any subject matter.

[3]Applicants note for the record that *Parvin* and *Witkowski* qualify as "prior art," if at all, under 35 U.S.C. § 102(e). Therefore, Applicants reserve the right to challenge the status of *Parvin* and *Witkowski* as proper references should such become necessary or desirable in Applicants' view at some time in the future. Accordingly, no argument in this paper should be construed as acquiescing in the "prior art" status of *Parvin* and *Witkowski*, and all such arguments are made simply assuming *arguendo* that the references qualify as prior art.

evaluated again, based at least on how many entries are in the circular list and how much time is needed to service the one or more channels corresponding to the entries in the circular list, (ii) determining a latency that represents how long the main memory will take to respond to a data request, (iii) determining a buffer time that represents how long data stored in the data reservoir maintained by the DMA engine will last for the channel, and (iv) determining that the channel requires service if the buffer time is less than the entry time and the latency. The method also includes servicing the channel by requesting channel data from the main memory to replenish the data reservoir if the channel requires service.

Applicants' invention, as claimed for example in independent method claim 8, additionally relates to a method for servicing memory requirements of one or more devices in a system having a main memory storing data for the one or more devices. The method includes generating a centralized data reservoir, by a direct memory access (DMA) engine that is external to and shared by the one or more devices, for consolidating one or more otherwise separate memory buffers within the one or more devices in order to reduce device buffer requirements. The data reservoir maintains a buffer for each of the one or more devices and the DMA engine implements DMA control logic so that DMA control logic need not be duplicated in each of the one or more devices. The DMA engine also determines whether a data request should be made to the main memory for each of the one or more devices. For each of the one or more devices requiring service for the data request, the DMA engine requests additional data to replenish each buffer in the data reservoir for each of the one or more devices from the main memory. The method further includes providing each of the one or more devices with access to each respective buffer in the data reservoir. Similar limitations may be found in independent system claim 37.

As noted above, the Office Action rejected independent claims 1, 8, and 37 under 35 U.S.C. § 102(e) as anticipated by *Parvin*. *Parvin* discloses a system for managing multiple DMA channels between a peripheral device and memory. Abstract; col. 10, ll. 13-15. Because having multiple DMA channels potentially increases the probability for bus conflicts, *Parvin* provides buffering for each DMA channel in the peripheral device. Col. 10, ll. 39-47. For example, in *Parvin* this buffering takes the form of a FIFO buffer 306 for an audio processing device 300 within an audio processing peripheral. Col. 12, ll. 4-5; Figure 13; col. 14, l. 61 – col. 4. A number of separate components within the peripheral device may share the FIFOs of the audio processing device. Col. 15, ll. 15-22; col. 16, ll. 25-46. A FIFO controller and a DMA

controller within the peripheral device maintain the FIFOs and manage the multiple DMA channels. Col. 16, ll. 47-62.

The FIFO controller monitors the input of data from the FIFOs and monitors trigger levels for the FIFOs so that when a trigger level is reached by a FIFO, the FIFO controller can pass a request for DMA access for the appropriate DMA channel to the DMA controller. Col. 16, ll. 47-54. The trigger level is set by the system CPU under the direction of the peripheral driver. *Id.* *Parvin* discloses the trigger level as simply a size/percentage of the FIFO buffer. Col. 12, ll. 16-56. For example, *Parvin* describes a FIFO buffer of 32 samples in depth for each of 48 DMA channels with a trigger level of 16 samples (half the buffer size). *Id.* Given a maximum bus latency of 4 microseconds, the 16 sample trigger level allows for 320 microseconds (at 20 microseconds per sample) before running out of data. *Id.* Accordingly, in the worst case, the 48th channel can wait more than 4 microsecond for each of 47 DMA channel requests that may come before it (i.e., 47 request at 4 microseconds each is only 188 microseconds, which is less than the 320 microseconds provided by the 16 sample trigger level).

In *Parvin*, once the trigger level is reached, a DMA request is generated—no determination is made with respect to the channel, based on its bandwidth requirements, the amount of data remaining for the channel, and when the channel will be evaluated again. Accordingly, Applicants respectfully submit that among other things, *Parvin* fails to teach, suggest, or motivate evaluating a channel associated with an entry in the circular list to determine whether the channel requires service by (i) determining an entry time representing how long until the channel will be evaluated again, based at least on how many entries are in the circular list and how much time is needed to service the one or more channels corresponding to the entries in the circular list, (ii) determining a latency representing how long the main memory will take to respond to a data request, (iii) determining a buffer time representing how long data stored in the data reservoir maintained by the DMA engine will last for the channel, and (iv) determining that the channel requires service if the buffer time is less than the entry time and the latency, as claimed for example in independent claim 1. Rather, as described above, *Parvin* makes a DMA request when the trigger level is reached, without considering whether the request could be delayed, given when the channel will be next evaluated, its bandwidth requirement, and the amount of data remaining. As a result, *Parvin* may make smaller and less efficient DMA requests, when it would be possible to make larger and more efficient DMA request by

practicing Applicants' invention, which may lead to larger buffer requirements in *Parvin* than are necessary. *See, e.g.,* Specification, p. 3, ll. 6-20; p. 5, l. 23 – p. 6, l. 13.

As discussed above, *Parvin* also discloses adding memory buffers and DMA logic to peripheral devices. *See, e.g.,* FIFOs 306, DMA controller 310, and FIFO controller 320 of Figure 13. As Applicants note in the Specification, a solution like *Parvin's* may result both in larger memory buffers than are necessary and unnecessary DMA control logic for peripheral devices. *See, e.g.,* Specification, p. 3, l. 21 0 p. 4, l. 4. Accordingly, Applicants respectfully submit that among other things, *Parvin* fails to teach, suggest, or motivate generating a centralized data reservoir, by a direct memory access (DMA) engine that is external to and shared by the one or more devices, for consolidating one or more otherwise separate memory buffers within the one or more devices in order to reduce device buffer requirements, the data reservoir maintaining a buffer for each of the one or more devices and the DMA engine implementing DMA control logic so that DMA control logic need not be duplicated in each of the one or more devices, wherein the DMA engine communicates with the main memory and the one or more devices communicate with the DMA engine, as claimed for example in independent claim 8. Similar limitations may be found in independent claim 37.

Applicants' invention, as claimed for example in independent method claim 27, further relates to a method for arbitrating data requests from one or more devices in a system that includes a main memory storing data for the one or more devices. The method includes creating an arbitration mechanism at a direct memory access (DMA) engine, selecting eligible devices from the one or more devices using the arbitration mechanism, and allowing the eligible devices to make data requests to the DMA engine for one channel of each of the eligible devices.

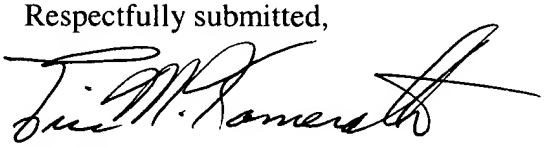
As noted above, the Office Action rejected independent claim 27 under 35 U.S.C. § 102(b) as anticipated by *Beck*. In particular, the Office Action asserts that *Beck's* rotating priority scheme anticipates independent claim 27. *Beck's* priority scheme is illustrated in Figures 12a and 12b. As shown, the scheme essentially moves the most recently serviced DMA channel to the lowest priority. Col. 32, ll. 11-56. *Beck*, however, makes no disclosure with respect to which devices are eligible to make a DMA request, rather *Beck* merely identifies a priority for various competing DMA channels. Accordingly, Applicants respectfully submit that among other things, *Beck* fails to teach, suggest, or motivate selecting eligible devices from one or more devices using an arbitration mechanism, and allowing the eligible devices to make data requests

to the DMA engine for one channel of each of the eligible devices, as claimed for example, in independent claim 27. In the Examiner's citation to *Beck*, it appears that all devices are eligible to make a DMA request.

Based on at least the foregoing reasons, Applicants respectfully submit that the cited art does not anticipate or make obvious Applicants' claimed invention. Accordingly, Applicants believe that all pending claim are now in condition for allowance.[4] In the event that the Examiner finds any remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, the Examiner is requested to contact one of the undersigned attorneys.

Dated this 19th day of January, 2004.

Respectfully submitted,



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[4]Applicants note for the record that any remaining rejections of record are now moot. Applicants, therefore, reserve the right to challenge any assertions in the Office Action with respect to the teachings of the prior art in the future.